PATENT
Docket No. P1571

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):	JENNIFER WANG MIKE BARSKY		
SERIAL NO.:	10/781,353	EXAMINER:	ANH D. MAI
FILED:	FEBRUARY 17, 2004	ART UNIT:	2814
FOR:	VIA FORMED IN POLYMER LAYER		

MAIL STOP AMENDMENT
COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

RESPONSE TO OFFICE ACTION
UNDER 37 C.F.R. § 1.116

To the Commissioner:

This letter is a Response to the Final Office Action dated January 13, 2006. The Applicants are respectfully requesting favorable consideration of the below submitted amendment and remarks under 37 C.F.R. § 1.116.

AMENDMENT

In the Claims: **Kindly amend Claims 21 and 22 as follows in the complete listing of claims. No new matter has been introduced.**

1. (withdrawn) A via etching process for a polymer layer deposited on a semiconductor substrate comprising said steps of:
placing a hard-mask on said polymer layer;
placing a photoresist mask on said hard-mask;
releasing a first fluoride gas into a chamber to etch a hard-mask opening for defining said via hole; and
releasing a second fluoride gas into said chamber to etch an exposed portion of said polymer layer defining said via hole with vertical sidewalls.

2. (withdrawn) A via etching process as recited in Claim 1, wherein said first fluoride gas comprises
trifluoromethane and argon.

3. (withdrawn) A via etching process as recited in Claim 1, wherein said first fluoride gas comprises a volume ratio of one part trifluoromethane to one part argon.

4. (withdrawn) A via etching process as recited in Claim 1, wherein said step of releasing first fluoride gas further includes applying bias power within the range of approximately 25 Watts to approximately 32 Watts.

5. (withdrawn) A via etching process as recited in Claim 1, wherein said step of releasing first fluoride gas further includes applying pulse-modulated power comprising inductively coupled plasma power within the range of approximately 725 Watts to approximately 755 Watts.

6. (withdrawn) A via etching process as recited in Claim 1, wherein said said step of

releasing first fluoride gas further includes for approximately three to seven minutes doing all the following: applying a first fluoride gas comprising an equal ratio of trifluoromethane and argon, applying a pressure of approximately 10 milli-Torr, applying a temperature of approximately 20 degrees C, applying pulse-modulated power comprising inductively coupled plasma power within the range of approximately 725 Watts to approximately 755 Watts, and applying bias power within the range of approximately 25 Watts to approximately 32 Watts.

7. (withdrawn) A via etching process as recited in Claim 1, wherein said second fluoride gas comprises Sulfur Hexafluoride and Oxygen.

8. (withdrawn) A via etching process as recited in Claim 1, wherein said second fluoride gas comprises Sulfur Hexafluoride and Oxygen, wherein said volume ratio of gases is 1 part Sulfur Hexafluoride to 3 parts Oxygen.

9. (withdrawn) A via etching process as recited in Claim 1, wherein said polymer layer etching step further comprises applying bias power within the range of approximately 57 Watts to approximately 62 Watts.

10. (withdrawn) A via etching process as recited in Claim 1, wherein step of releasing a second fluoride gas further includes applying pulse-modulated power comprising inductively coupled plasma power within the range of approximately 475 Watts to approximately 505 Watts.

11. (withdrawn) A via etching process as recited in Claim 1, wherein step of releasing a second fluoride gas further includes for approximately one and half minutes to six minutes doing all the following: applying a second fluoride gas comprising Sulfur Hexafluoride and Oxygen, wherein said ratio of gases is 1 part Sulfur Hexafluoride to 3 parts Oxygen with an associated pressure of approximately 5 milli-Torr, applying temperature of approximately 20 degrees C, applying pulse-modulated power comprising inductively coupled plasma power with the range of approximately 475

Watts to approximately 505 Watts, and applying bias power comprising a bias power with the range of approximately 25 Watts to approximately 32 Watts.

12. (withdrawn) A via etching process as recited in Claim 1, wherein said polymer layer is benzocyclobutene polymer.

13. (withdrawn) A via etching process as recited in Claim 1, wherein said polymer layer is a material with a dielectric constant less than 3.

14. (withdrawn) An etch process as recited in Claim1, wherein said semiconductor substrate is chosen from the group consisting of Indium Phosphide and Gallium Arsenide.

15. (withdrawn) A via etching process for a polymer layer on a semiconductor substrate comprising the steps of:

placing in a chamber said semiconductor substrate including a polymer layer defining a sub-micron wide via-opening deposited on said semiconductor substrate, and a hard-mask defining said sub-micron wide via-opening deposited on said polymer layer;

releasing a third fluoride gas into said chamber;

applying bias power within the range of approximately 105 Watts to approximately 120 Watts;

applying pulse-modulated power within the range of approximately 725 Watts to approximately 755 Watts;

pressurizing said third fluoride gas within a range of approximately 5 milli-Torr to approximately 20 milli-Torr; and

continuing the above steps until etching said hard-mark and an exposed portion of said polymer layer proximal to said sub-micron wide via-opening creating tapered sidewalls.

16. (withdrawn) A via etching process as recited in Claim 15, wherein said third fluoride

gas comprises trifluoromethane and argon.

17. (withdrawn) A via etching process as recited in Claim 15, wherein said third fluoride gas comprises a volume ratio of one part trifluoromethane to one part argon.

18. (withdrawn) A via etching process as recited in Claim 15, wherein said continuing the above steps within the range of approximately three minutes to approximately seven minutes.

19. (withdrawn) A via etching process as recited in Claim 15, wherein said polymer layer is benzocyclobutene polymer.

20. (withdrawn) A via etching process as recited in Claim 15, wherein said polymer layer is a material with a dielectric constant less than 3 and has an etch rate 10 times slower than that of said hard-mask layer.

21. (currently amended) A device including a via produced by the process comprising the steps of:

placing a hard-mask on a polymer layer;

placing a photoresist mask on said hard-mask;

releasing a first fluoride gas into a chamber to etch a hard-mask opening for defining a via hole; and

releasing a second fluoride gas into said chamber to etch an exposed portion of said polymer layer defining said via hole with at least one vertical sidewall,

whereby the via hole comprises an aspect ratio which is greater than 1, and is of substantially the same diameter throughout the depth of the via hole.

22. (currently amended) A device including a via produced by the process comprising the steps of:

placing, in a chamber, a semiconductor substrate including a polymer layer defining a submicron wide via-opening deposited on said semiconductor

substrate, and a hard-mask defining said submicron wide via-opening deposited on said polymer layer;

releasing a ~~third~~ fluoride gas into said chamber;

applying bias power within the range of approximately 105 Watts to approximately 120 Watts;

applying pulse-modulated power within the range of approximately 725 Watts to approximately 755 Watts;

pressurizing said third fluoride gas within a range of approximately 5 milliTorr to approximately 20 milliTorr; and

continuing the above steps until etching said hard-mark and an exposed portion of said polymer layer proximal to said submicron wide via-opening thereby creating at least one tapered sidewall within a via hole,

whereby the via hole ~~opening~~ comprises an aspect ratio which is greater than 1, and is of substantially the same diameter throughout the depth of the via hole.

REMARKS

I. Introductory Remarks.

The Applicants hereby thank the Examiner for the observations in the outstanding Office Action mailed January 13, 2006 and the telephone conversation on May 9, 2006. Method Claims 1-20 are non-elected and are withdrawn from consideration. Device Claims 21-22 are pending and are herein amended to better encompass the full scope and breadth of the present invention, notwithstanding the Applicants' belief that the claims would have been allowable as originally filed. Reconsideration of the present application in light of the foregoing amendment and following remarks is respectfully requested.

II. Rejection of Claim 21 under 35 U.S.C. §103(a).

Claim 21 has been rejected, under 35 U.S.C. §103(a) as being unpatentable over Yu et al (U.S. Patent No. 6,004,883) of record in view of Lin (U.S. Pub. No. 2002/0068441). The Applicants hereby respectfully request reconsideration of this ground of rejection in light of the following remarks. Independent device Claim 21 is herein amended by inserting the following language regarding the via hole, "is of substantially the same diameter throughout the depth of the via hole" which is fully supported by the originally filed Specification (numbered Paras. 23, 26, 27, 30, and 37).

Addressing the cited art, Yu merely teaches a method for forming a via whereby the resulting aperture comprises a second trench corresponding with a first trench and at least a portion of a first via. The method taught by Yu is unable to etch a deep via hole having substantially the same diameter throughout the depth of the via without requiring another exorbitant photoresist mask set which adds a step and interrupts the etching process.

The method taught by Yu involves a first patterned dielectric layer that defines a via. After this first dielectric layer that is non-etchable is deposited, a second dielectric layer is blanketed to fill the via, whereby this second dielectric layer is susceptible to etching. In

Figure 2 of Yu, the blanket hard mask that overlays the second dielectric layer is patterned to form a series of patterned first hard mask layers, which is not susceptible to etching. Upon the blanket hard mask layer a patterned photoresist layer is laid which leaves exposed a portion of the blanket hard mask layer greater than an areal dimension of the via and at least partially overlapping the areal dimension of the via. The first plasma etch method works on the blanket hard mask layer to form a patterned hard mask layer defining a first trench. Next a second plasma etch method is employed to form a patterned second dielectric layer having an aperture formed therethrough.

Yu teaches how to form an aperture that comprises a second trench corresponding with a first trench and at least a portion of a first via. This process and subsequent aperture structure often results in overlapping vias, which damages adjacent device features such as resistors, capacitive layers, other via holes, or other transistor layers. The apertures formed are substantially structurally different than the vias of Claim 21.

The vias created by Claim 21 are dimensionally accurate micron and sub-micron via holes of substantially the same diameter throughout the depth of the via hole due to the prescribed method of the present invention. This method comprises depositing a polymer layer on a semiconductor substrate, depositing a hard-mask on the polymer layer, and depositing a photoresist mask on the hard-mask. A first fluoride gas is released into a chamber to etch a hard-mask opening that defines a via hole, and then subsequently releasing a second fluoride gas into the chamber to etch the polymer layer.

Lin does disclose a via with an aspect ratio greater than one. However, since Yu does not anticipate the present invention for the reasons stated above, adding Lin merely for the aspect ratio would still not accomplish the structure of the claimed device. Therefore, the Applicants respectfully request that this ground for rejection on this basis be withdrawn and that Claim 21 be passed to allowance.

III. Rejection of Claim 22 under 35 U.S.C. §103(a).

Claim 22 has been rejected, under 35 U.S.C. §103(a) as being unpatentable over Schuck, III et al (U.S. Patent No. 5,868,951) of record in view of Lin (U.S. Pub. No. 2002/0068441). The Applicants hereby respectfully request reconsideration of this ground of rejection in light of the following remarks. Independent device Claim 22 is herein amended by inserting the following language regarding the via hole, "is of substantially the same diameter throughout the depth of the via hole" which is fully supported by the originally filed Specification (numbered Paras. 23, 26, 27, 30, 31, 32, 36 and 37).

Addressing the cited art, Schuck merely shows vias that are opened in the cured polymeric resin to each pixel. Figure 4A of Schuck shows tapering of the entire via. Nowhere does Schuck teach the claimed method of producing via holes in a thick polymer layer having substantially the same diameter throughout the depth of the via hole, especially having a last step of tapering the via hole at the via-opening. The apertures formed by Schuck are substantially structurally different than the vias of Claim 22.

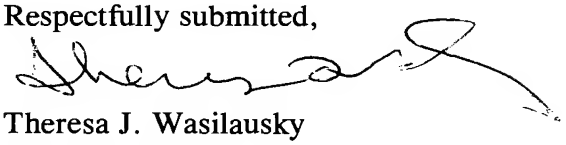
The vias created by Claim 22 are dimensionally accurate micron and sub-micron via holes of substantially the same diameter throughout the depth of the via hole, with tapering at the via-opening due to the prescribed method of the present invention. This method of a via etching for a polymer layer on a semiconductor substrate comprises, depositing a polymer layer defining a submicron via opening on the semiconductor substrate and depositing a hard-mask defining the submicron wide via-opening on the polymer layer. A third fluoride gas is released into the chamber so that the hard-mask is etched away along with an exposed portion of the polymer layer proximal to the submicron wide via-opening, to create tapered sidewalls within a via hole having substantially the same diameter throughout the length of the via hole.

Lin does disclose a via with an aspect ratio greater than one. However, since Schuck does not anticipate the present invention for the reasons stated above, adding Lin merely for the aspect ratio would still not accomplish the structure of the claimed device. Therefore, the Applicants respectfully request that this ground for rejection on this basis be withdrawn and that Claim 22 be passed to allowance.

CONCLUSION

The Applicants would like to thank the Examiner again for the telephone conversation of May 9, 2006. Applicants respectfully request that the device Claims of 21-22 as herein amended to better encompass the full scope and breadth of the present invention be reconsidered in light of the foregoing amendment and remarks, notwithstanding Applicants' belief that the claims would have been allowable as originally filed. The Examiner is further cordially invited to telephone the undersigned for any reason, which would advance the allowance of the pending claims.

Respectfully submitted,



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